DATA SHEET

PCA84C922; PCA84C923
Microcontrollers for universal infrared remote transmitter applications

Product specification
File under Integrated Circuits, IC14

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CONTENTS

1 FEATURES

- 84CXXX CPU
- ROM, RAM, I/O and keypad configurations are device dependent; see Table 1
- Two test inputs: T0 and T1
- 3 single-level vectored interrupt sources:
  - external (T0/$\overline{\text{INT}}$ and Port 1, for keypad press Wake-up function)
  - Timer/counter (TI)
  - Hardware Modulator interrupt
- 8-bit programmable timer/counter with 5-bit prescaler
- Power saving Idle and Stop modes
- Low power operation: 2 V
- Hardware Modulator
- Watchdog timer
- On-chip oscillator: 1 to 6 MHz
- Single supply voltage: 2.0 to 5.5 V
- Operating temperature: –20 to +70 °C
- Available packages: SO24, SO28, VSO56 and SDIP24.

2 GENERAL DESCRIPTION

The PCA84C922A, PCA84C922C, PCA84C923A, PCA84C923C and PCA84C923D are members of the PCF84CXXXA CMOS family of microcontrollers and have been designed for use in universal infrared remote commander applications. The term PCA84C92X is used throughout this data sheet to refer to all devices in the range, differences between devices are shown in Table 1 and also highlighted in the text. In addition to the common functions of the PCF84CXXXA family of microcontrollers the PCA84C92X also provides:

- a Hardware Modulator that generates programmable pulse trains for driving an infrared LED
- an on-chip Coding Table specifically for the storage of code data
- a modified interrupt architecture that will wake-up the CPU from the Idle or Stop modes when any key is pressed
- a Watchdog Timer to prevent CPU lock-up.

The PCA84C923D has been designed as the emulation chip for both the PCA84C92X and the PCA84CX22 range of microcontrollers (both ranges being pin compatible).

Table 1 The PCA84C92X range of microcontrollers

FUNCTION	PCA84C923D	PCA84C923C	PCA84C923A	PCA84C922C	PCA84C922A
System ROM	8 kbytes	8 kbytes	8 kbytes	8 kbytes	8 kbytes
System RAM	256 bytes	256 bytes	256 bytes	128 bytes	128 bytes
Coding Table ROM	16 kbytes	16 kbytes	16 kbytes	8 kbytes	8 kbytes
Coding Table extension	up to 64 kbytes	no	no	no	no
Maximum number of keys	189	117	81	117	81
I/O	36	20	16	20	16
Emulation device	PCA84C923D	PCA84C923D	PCA84C923D	PCA84C923D	PCA84C923D
Package	VSO56	SO28	SO24 and SDIP24	SO28	SO24 and SDIP24

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA84C922AP	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA84C922AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA84C922CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCA84C923AP	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA84C923AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA84C923CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCA84C923DT	VSO56	plastic very small outline package; 56 leads	SOT190-1

4 BLOCK DIAGRAMS

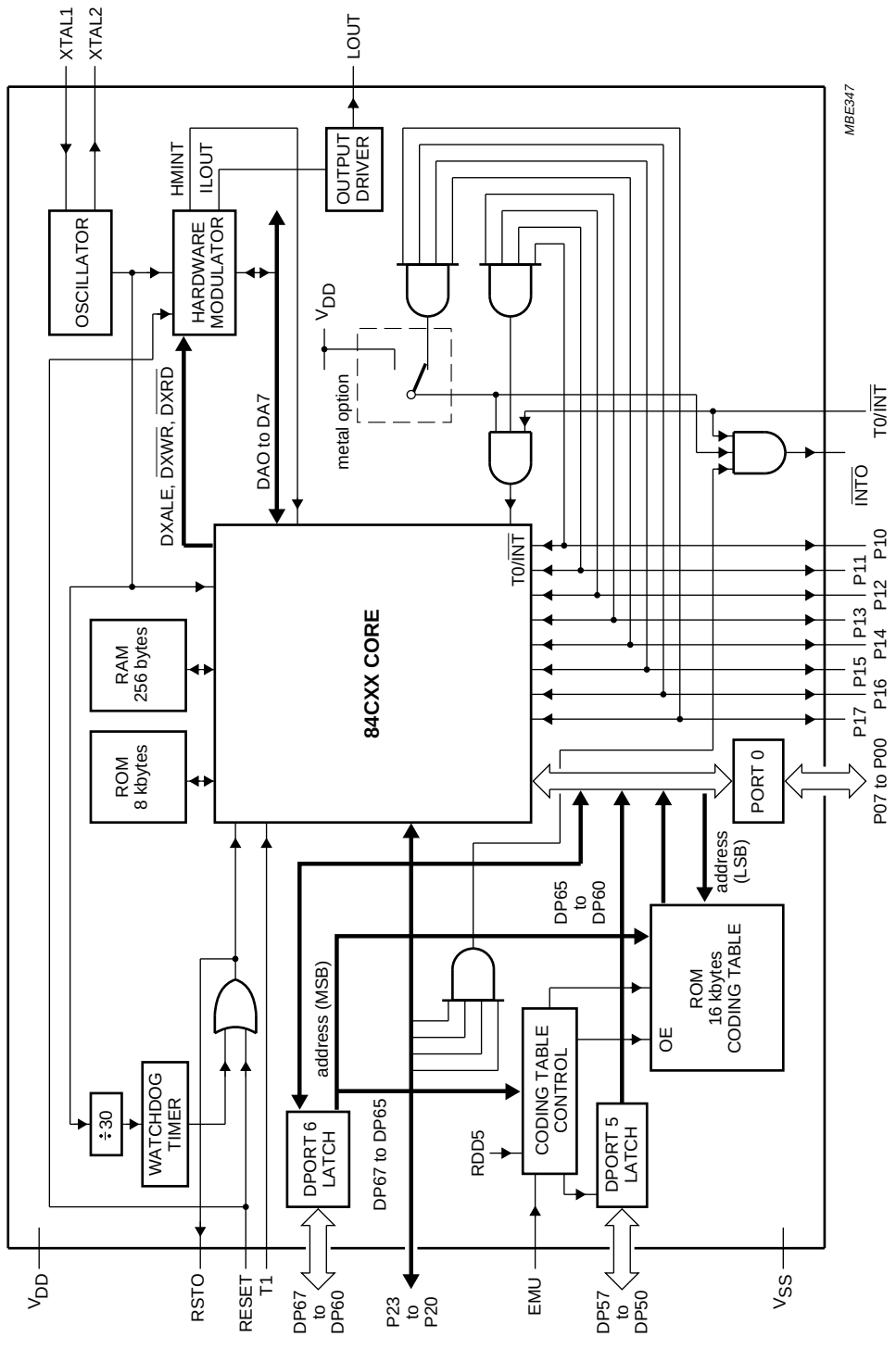


Fig.1 Block diagram - PCA84C923D.

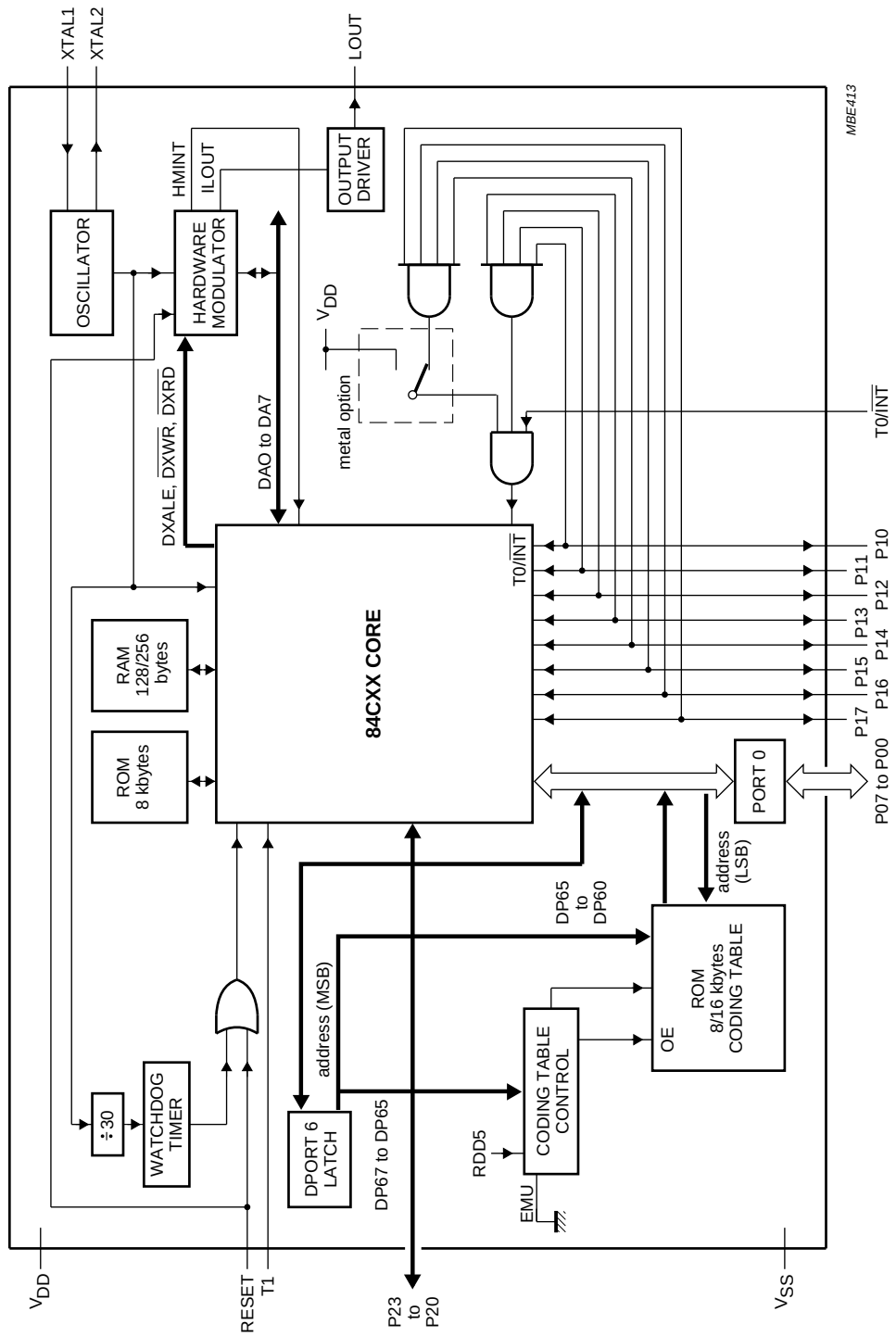


Fig.2 Block diagram - PCA84C922C and PCA84C923C.

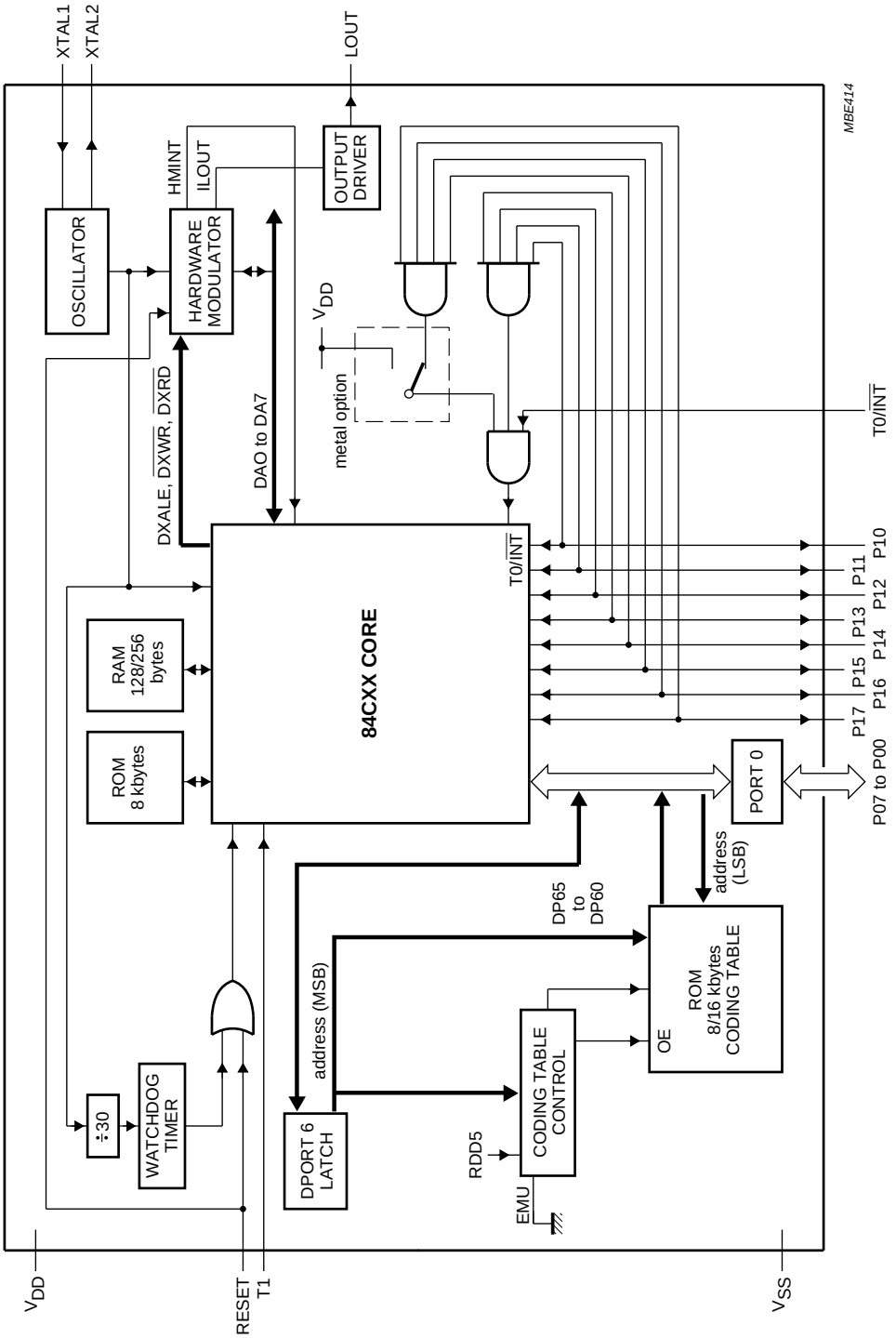


Fig.3 Block diagram - PCA84C922A and PCA84C923A.

5 PINNING INFORMATION

5.1 Pinning

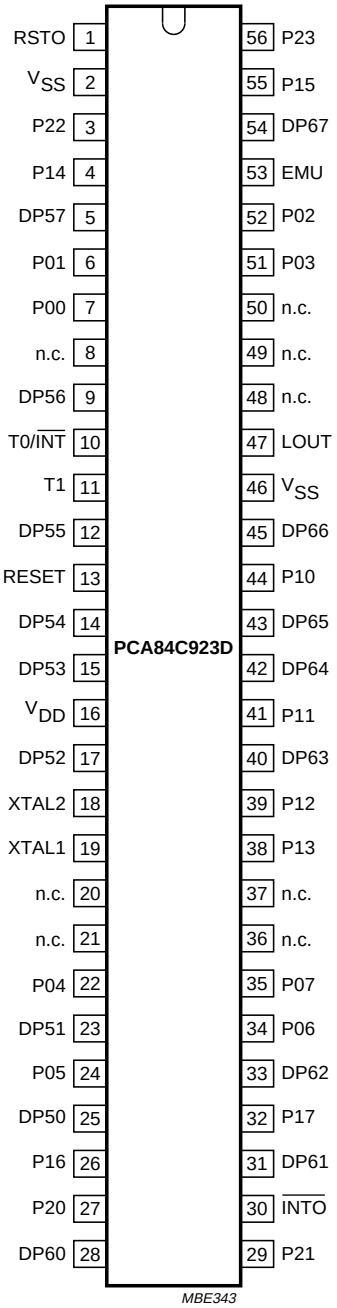


Fig.4 Pin configuration of PCA84C923D (VSO56).

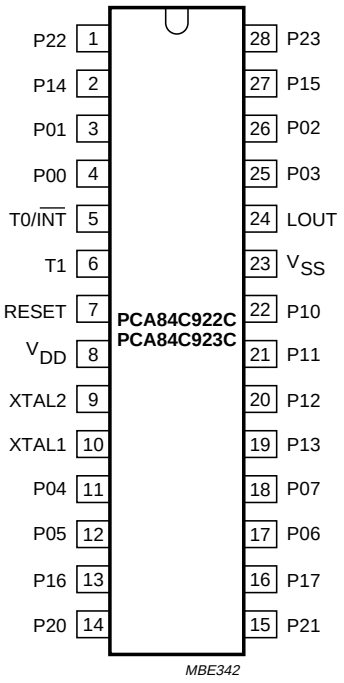


Fig.5 Pin configuration of PCA84C922C (SO28) and PCA84C923C (SO28).

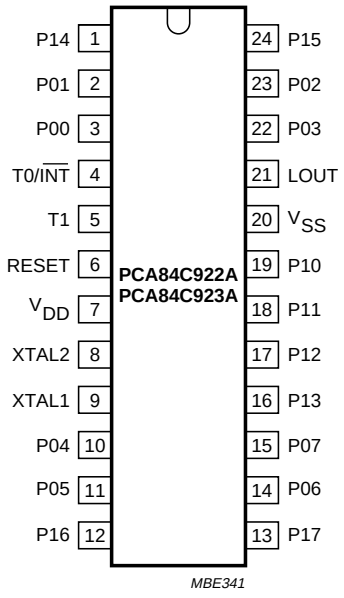


Fig.6 Pin configuration of PCA84C922A (SO24/SDIP24) and PCA84C923A (SO24/SDIP24).

5.2 Pin description

Table 2 PCA84C923D (VS056)

SYMBOL	PIN	DESCRIPTION
P00 to P07	7, 6, 52, 51, 22, 24, 34 and 35	Standard I/O Port lines, generally used for keypad scanning or for LSB address lines of coding table.
P10	44	Port line 10 or emulation $\overline{\text{DXWR}}$ signal input.
P11	41	Port line 11 or emulation $\overline{\text{DXRD}}$ signal input.
P12	39	Port line 12 or emulation DXALE signal input.
P13	38	Port line 13 or emulation $\overline{\text{EXDI}}$ signal input.
P14 to P17	4, 55, 26 and 32	Standard I/O port lines, generally used for keypad sensing, the wake-up function can be removed by mask option.
P20 to P23	27, 29, 3 and 56	Standard I/O port lines with 10 mA sink capability.
DP50 to DP57	25, 23, 17, 15, 14, 12, 9 and 5	Standard I/O port lines, generally used for the data bus of Coding Table.
DP60 to DP67	28, 31, 33, 40, 42, 43, 45 and 54	Standard I/O Port lines, generally used for keypad scanning or for MSB address lines of Coding Table.
RSTO	1	Used for emulation purposes only. This output is the result of the OR operation carried out internally on the RESET input and the Watchdog Timer reset and is connected to the RESET pin of the 84C00.
T0/$\overline{\text{INT}}$	10	Test pin T0 or external interrupt input.
T1	11	Test pin T1 or timer/counter input (T1).
RESET	13	Active HIGH reset pin; normally connected to V_{SS} as Power-on-reset serves the same function.
XTAL2	18	Crystal or ceramic resonator or LC oscillator connections.
XTAL1	19	
$\overline{\text{INTO}}$	30	Used for emulation purposes only and is connected to the T0/$\overline{\text{INT}}$ pin of the 84C00.
LOUT	47	Pulse train output pin, capable of sinking 30 mA.
EMU	53	Emulation mode control pin; for normal operation this pin is connected to V_{SS}.
V_{DD}	16	Power supply.
V_{SS}	2 and 46	Ground.

Table 3 PCA84C922C (SO28) and PCA84C923C (SO28)

SYMBOL	PIN	DESCRIPTION
P00 to P07	4, 3, 26, 25, 11, 12, 17, 18	Standard I/O port lines, generally used for keypad scanning or for LSB address byte of code data.
P10 to P17	22, 21, 20, 19, 2, 27, 13, 16	Standard I/O port lines, generally used for keypad sensing, the wake-up function of P14 to P17 can be removed by mask option.
P20 to P23	14, 15, 1, 28	Standard I/O port lines with 10 mA sink capability.
T0/$\overline{\text{INT}}$	5	Test pin T0 or external interrupt input.
T1	6	Test pin T1 or timer/counter input (T1).
RESET	7	Active HIGH reset pin; normally connected to V_{SS} as Power-on-reset serves the same function.
XTAL2	9	Crystal or ceramic resonator or LC oscillator connections.
XTAL1	10	
LOUT	24	Pulse train output pin, capable of sinking 30 mA.
V_{DD}	8	Power supply.
V_{SS}	23	Ground.

Table 4 PCA84C922A (SO24/SDIP24) and PCA84C923A (SO24/SDIP24)

SYMBOL	PIN	DESCRIPTION
P00 to P07	3, 2, 23, 22, 10, 11, 14, 15	Standard I/O port lines, generally used for keypad scanning or for LSB address byte of code data.
P10 to P17	19,18, 17, 16, 1, 24,12,13	Standard I/O port lines, generally used for keypad sensing, the wake-up function of P14 to P17 can be removed by mask option.
T0/$\overline{\text{INT}}$	4	Test pin T0 or external interrupt input.
T1	5	Test pin T1 or timer/counter input (T1).
RESET	6	Active HIGH reset pin; normally connected to V_{SS} as Power-on-reset serves the same function.
XTAL2	8	Crystal or ceramic resonator or LC oscillator connections.
XTAL1	9	
LOUT	21	Pulse train output pin, capable of sinking 30 mA.
V_{DD}	7	Power supply.
V_{SS}	20	Ground.

6 GENERAL OPERATION DESCRIPTION

The main application for the PCA84C92X is as a universal infrared remote control commander and in this role the PCA84C92X offers the complete solution in one chip.

The PCA84C92X can be programmed to generate code data that conforms to any protocol (Philips, NEC, RCA, Thomson and Siemens etc.) and is suitable for use in the remote control of TVs, VCRs, audio equipment, air-conditioning systems and in many other applications.

The ability of the PCA84C923D to access external memory and therefore support more protocols, makes it an extremely versatile device.

6.1 System selection

Different systems (TV or VCR etc) can be controlled using one universal infrared remote control commander; switches can be used to select a specific system. However, the PCA84C92X provides pin T1 for system selection purposes and software is used to detect the specific system. Port lines P14 to P17 can also be used for system selection if their wake-up functions have not been selected as a mask option.

When no key is pressed the scan lines (Port 0) can be programmed HIGH and the sense lines (Port 1) programmed LOW. If a diode is connected between a sense line and scan line then the scan line will be pulled LOW and this can be detected by a read operation to Port 0.

6.2 Key scanning

Port lines P10 to P17 and T0/$\overline{\text{INT}}$ have been designed to be used as key sense lines. However, if the wake-up option is not selected for ports P14 to P17 then these can be used as general I/O lines.

Port lines P00 to P07, P20 to P23 and DP60 to DP67 can be used as key scan lines or general I/O ports. Derivative Port 6 also provides the High byte address for the Coding Table, even when used as scan lines.

After a Power-on-reset, the scan lines are set LOW and the sense lines HIGH. If the system has entered the Stop mode (by software) then when any key is depressed an external interrupt will be generated and the system will be woken-up.

If the external interrupt was enabled (by using the ‘EN I’ instruction) before the Stop mode was entered, then when the CPU is woken-up, the instruction that follows the STOP instruction will be executed before diverting to the interrupt routine at vector address 03H. However, if the interrupt was not enabled before the Stop mode was entered, then when the CPU is woken-up the instruction that follows the STOP instruction will be executed.

6.3 Accessing command code

When any key is depressed its function and operation protocol are determined, then the command code is read. If the command code is stored in system ROM it can be accessed using the ‘MOVP A,@A’ instruction. If the command code resides in Coding Table ROM it can be accessed by writing the address to DP60 to DP67 (High byte) and P00 to P07 (Low byte) and then reading the data from DP50 to DP57.

In Normal mode, if the Coding Table address is within the 0000 to 1FFFH range for PCA84C922 devices, or within the 0000 to 3FFFH range for PCA84C923 devices, then the internal Coding Table will be accessed when Derivative Port 5 (address 05H) is read.

In the Normal mode only the PCA84C923D has the ability to access external memory. If the Coding Table address is greater than 3FFFH then the external memory will be accessed when Derivative Port 5 (terminal) is read.

When the PCA84C923D is used in the Emulation mode, when Derivative Port 5 is read, data will always be read from DP50 to DP57 terminals. Therefore, the internal Coding Table ROM can be emulated when the PCA84C923D and the bond-out chip PCF84C00 are used.

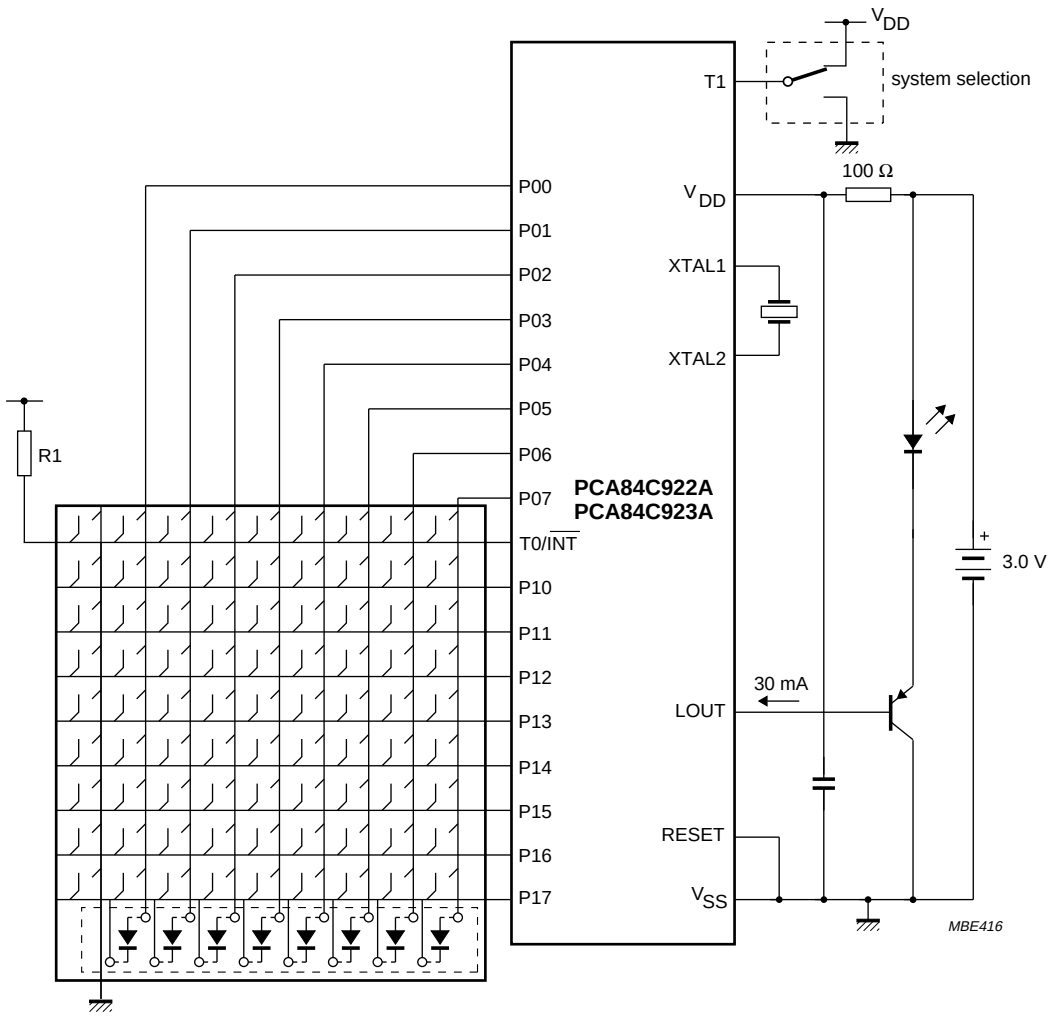


Fig.7 Typical Remote Control Transmitter application using the PCA84C922A or PCA84C923A.

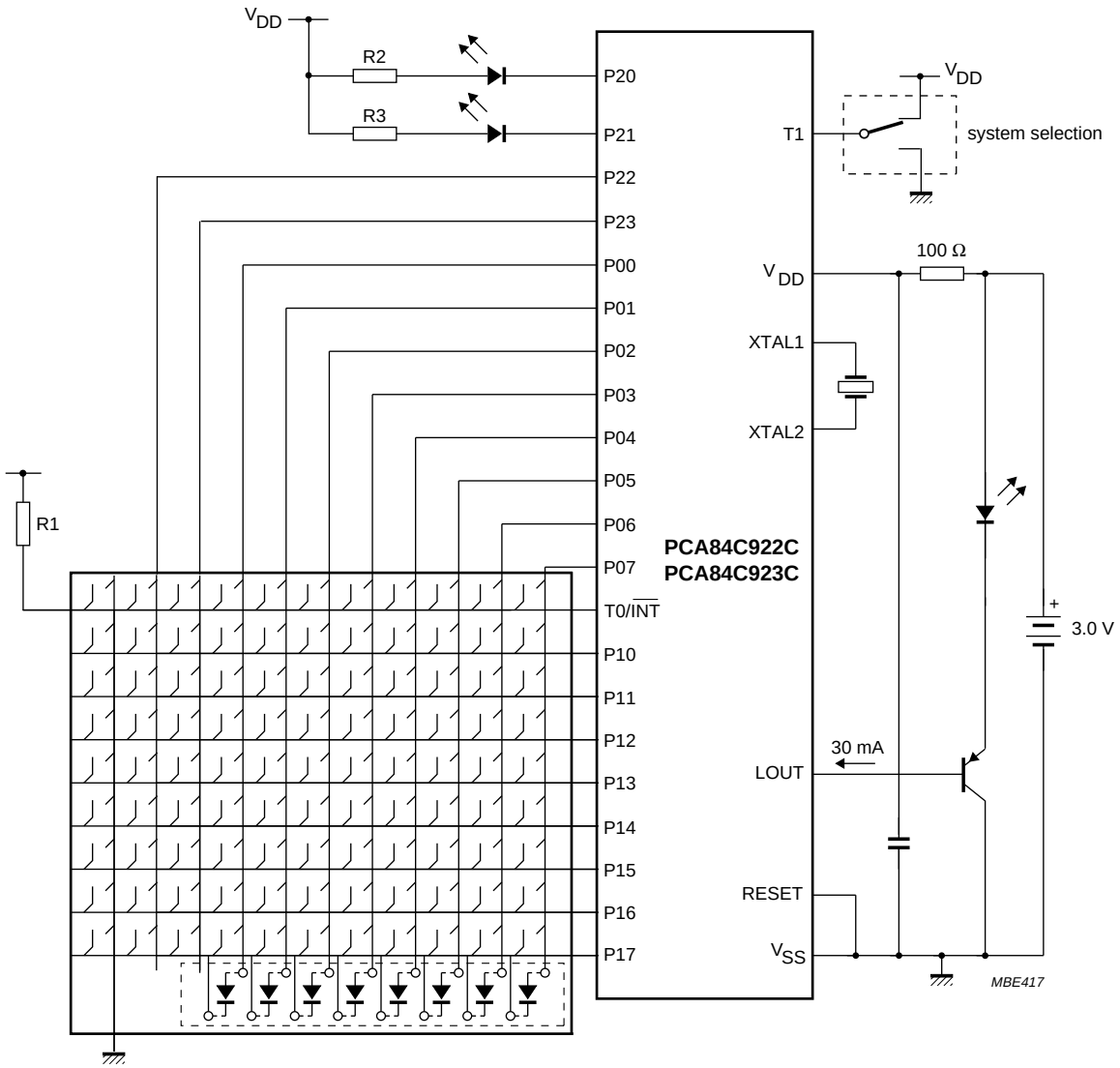


Fig.8 Typical Remote Control Transmitter application using the PCA84C922C or PCA84C923C.

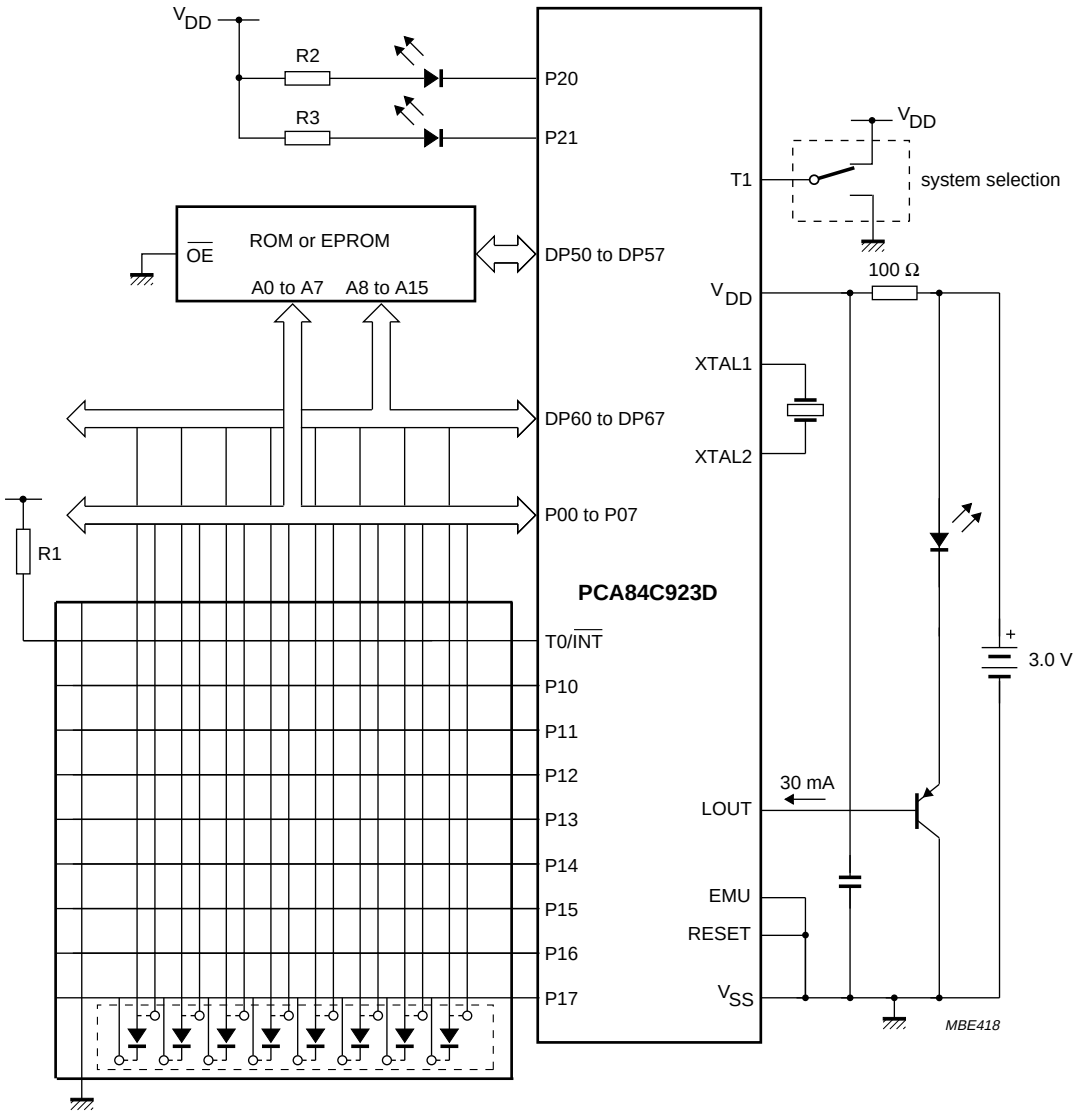


Fig.9 Typical Remote Control Transmitter application using the PCA84C923D.

7 HARDWARE MODULATOR

The Hardware Modulator used in the PCA84C92X is the same as the Hardware modulator used in the PCA84CX22 range of microcontrollers.

The function of the Hardware Modulator is to generate a coded pulse train which is subsequently converted into an infrared signal by an IR-LED. It is this coded IR signal that controls the remote equipment. The number of pulses in the pulse train, the time between pulse train bursts and the duty cycle of a pulse are all programmable. A typical pulse train is shown in Fig.10.

The block diagram of the Hardware Modulator is shown in Fig.14 and comprises:

- An 8-bit ON-time Register
- An 8-bit OFF-time Register
- An 8-bit Control Register
- A Pulse Timer
- A 10-bit Pulse Counter
- Control logic.

These are described in detail in Sections 7.1 to 7.5.

7.1 ON-time Register

The duty cycle of the pulse is determined by the contents of the ON-time and OFF-time Registers. The ON-time Register controls the active or ON period of the pulse; the OFF-time Register controls the inactive or OFF period of the cycle.

The 8-bit ON-time Register resides at address 00H and is loaded by software. The decimal value of its contents plus 2, determines the number of oscillator cycles that the LOUT pin is active. The active period of LOUT can be calculated as follows:

$$t_{ON} = \frac{(\text{decimal value held in ON-time Register} + 2)}{f_{osc}}$$

7.2 OFF-time Register

This 8-bit register resides at address 01H and is loaded by software. The decimal value of its contents plus 2, determines the number of oscillator cycles that the LOUT pin is inactive.

The inactive period of LOUT can be calculated as follows:

$$t_{OFF} = \frac{(\text{decimal value held in OFF-time Register} + 2)}{f_{osc}}$$

7.3 Pulse Timer

The contents of the ON-time and OFF-time Registers are loaded alternately into the Pulse Timer. When loaded the Pulse Timer contents are decremented by ‘1’ every oscillator cycle and upon reaching zero the Pulse Timer will be reloaded with the contents of the other register.

7.4 Pulse Counter

The 10-bit Pulse Counter actually consists of two registers: the 2-bit Pulse Counter High Register that resides at address 04H, and the 8-bit Pulse Counter Low Register that resides at address 02H.

The Pulse Counter is loaded by software; its contents determine the number of pulses in a specific pulse train.

7.5 Hardware Modulator Control Register (HMCTL)

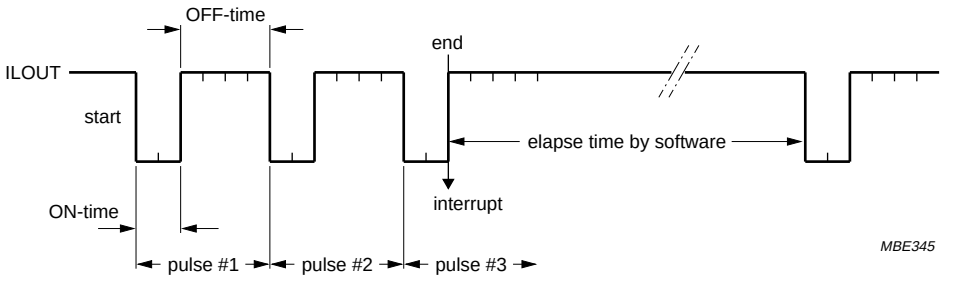
The characteristics of the pulse train are initially determined by the contents of the ON-time Register, the OFF-time Register and the Pulse Counter; however, the HMCTL Register allows these characteristics to be modified. The Watchdog Timer and derivative interrupt flag are reset via this register.

Table 5 Hardware Control Register (address 03H)

7	6	5	4	3	2	1	0
–	–	–	WRES	Rint	PWM	LgP	HF

Table 6 Description of the HMCTL bits

BIT	SYMBOL	DESCRIPTION
7 to 5	–	These three bits are reserved.
4	WRES	Reset Watchdog Timer. This is not a flip-flop in the register and can only be written to. If a logic 1 is written to this bit the Watchdog Timer is reset.
3	Rint	Reset interrupt. When Rint = 1; the interrupt flag that was set by the derivative logic is cleared. The Hardware Modulator can only be restarted after the interrupt flag is cleared; this avoids a second interrupt being generated before the first one has been serviced.
2	PWM	Pulse Width Modulation. When PWM = 1 and LgP = 0; the Pulse Counter Register is ignored and a continuous pulse train is generated, this is shown in Fig.13.
1	LgP	Long Pulse. When LgP = 1; the contents of the OFF-time Register are ignored. A single pulse is generated; its pulse width being determined as shown below. $\text{Pulse width} = (\text{Contents of ON-time Register} + 2) \times (\text{number of pulses}) \times \frac{1}{f_{osc}}$ If HF = 1; this pulse is modulated with a frequency $\frac{1}{4}f_{osc}$, this is shown in Fig.12.
0	HF	High Frequency. When HF = 1; the ON-time part of the generated pulse is modulated with a frequency $\frac{1}{4}f_{osc}$, this is shown as CASE 2 in Figs 11 and 12.



ON-time = 2 (on-time register = 0) OFF-time = 4 (off-time register = 2) number of pulses = 3

Fig.10 Example of ILOUT pulse train.

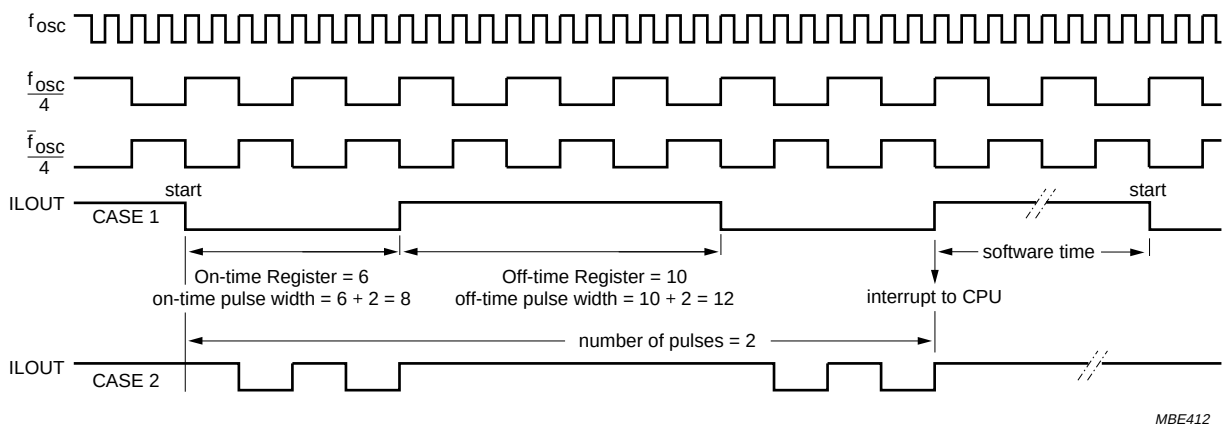


Fig.11 CASE 1 shows a typical pulse train; CASE 2 shows the same pulse train after being modulated with a frequency of $\frac{1}{4}f_{osc}$ (HF = 1).

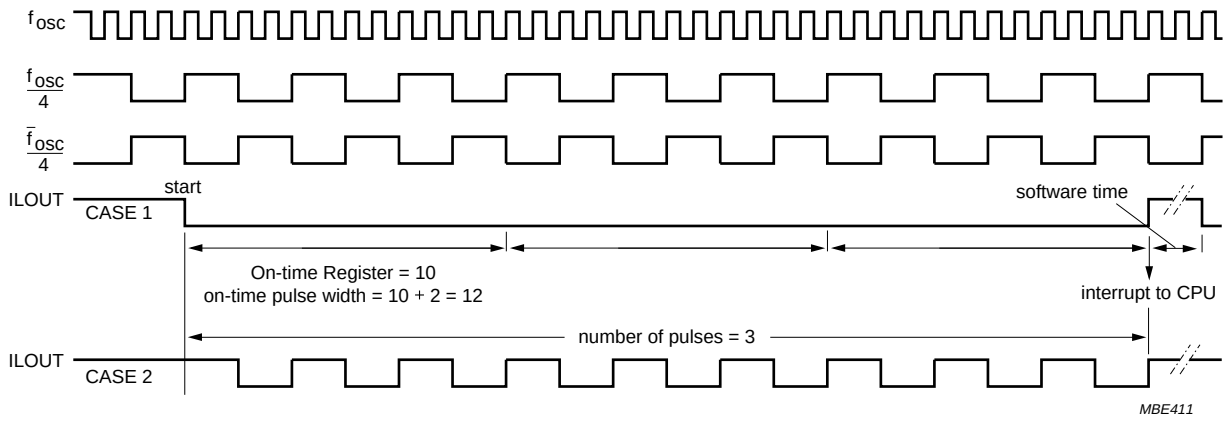


Fig.12 CASE 1 shows a typical long pulse; CASE 2 shows the same long pulse after being modulated with a frequency of $\frac{1}{4}f_{osc}$ (HF = 1).

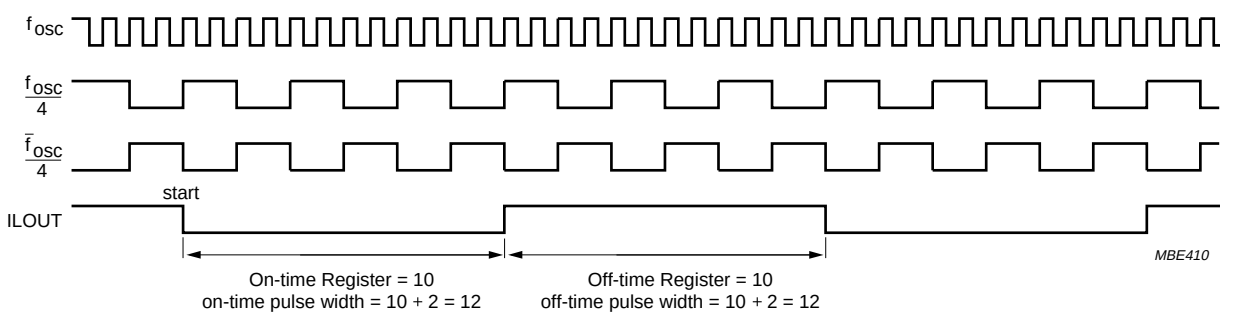


Fig.13 Continous pulse train (PWM = 1).

7.6 Operation of the Hardware Modulator

The ON-time, OFF-time, Pulse Counter High and Pulse Counter Low registers are loaded by software.

As soon as the Pulse Counter Low Register is loaded the Hardware Modulator is started and LOUT becomes active (LOW). Simultaneously, the contents of the ON-time Register are loaded into the Pulse Timer which is then decremented by '1' every oscillator clock cycle. When the value held in the Pulse Timer becomes zero the contents of the Pulse Counter are decremented by '1' and LOUT becomes inactive (HIGH).

The contents of the OFF-time Register are now loaded into the Pulse Timer which is decremented by '1' every oscillator clock cycle. When the value held in the Pulse Timer becomes zero, LOUT becomes active (LOW). One pulse cycle has now been generated.

The process of alternately loading the contents of the ON-time Register and OFF-time Register into the Pulse Timer continues until the contents of the Pulse Counter become zero. When this occurs $\overline{\text{EXDI}}$ is asserted; an interrupt to the CPU is generated and the interrupt flag is raised stopping the operation of the Hardware Modulator. The programmed pulse train has now been generated.

The Hardware Modulator can only be restarted after the interrupt flag has been cleared. The interrupt flag is cleared by writing a logic 1 to the Rint bit in the Hardware Modulator Control Register.

The time delay between two pulse trains is determined by software.

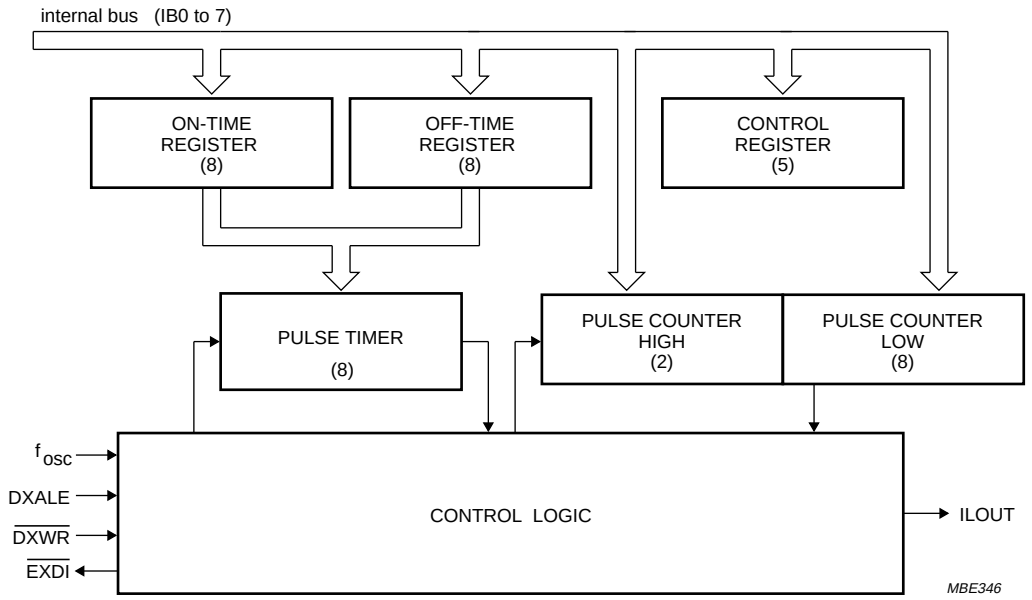


Fig.14 Block diagram of the Hardware Modulator.

8 CODING TABLE

The code data transmitted from the LOUT output when any key is depressed, is stored in a memory area known as the Coding Table. The PCA84C92X range of microcontrollers have on-chip ROM specifically for this use (system ROM may also be used). The Coding Table is addressed via Port 0 (the Low byte address) and Derivative Port 6 latch (the High byte address).

The PCA84C922 range of devices have 8 kbytes of ROM for use as a Coding Table and when accessing this internal memory, address lines DP65 to DP67 must be LOW.

The PCA84C923 range of devices have 16 kbytes of ROM for use as a Coding Table and when accessing this internal memory, address lines DP66 and DP67 must be LOW.

The Coding Table memory size for the PCA84C923D however, can be extended up to 64 kbytes by adding external memory (ROM or EPROM). The external memory data bus is connected to Derivative Port 5. Accessing the internal or external Coding Tables of the PCA84C923D is described below.

- In the Normal mode (EMU pin LOW)
  - When Derivative Port 5 terminal is read, if the address lines DP66 and DP67 are LOW, the address will be within the internal memory boundary, and the internal Coding Table will be accessed.
  - When Derivative Port 5 terminal is read, if either of the address lines DP66 or DP67 is HIGH, the address will be outside the internal memory boundary and the external memory will be accessed. The data at Derivative Port 5 terminal will then be read.
- In the Emulation mode (EMU pin HIGH)
  - When Derivative Port 5 terminal is read, external memory will always be accessed. In this situation, Derivative Port 5 latch cannot be read.

8.1 Accessing the Coding Table

The procedure for accessing the Coding Table follows:

1. Set all sense lines to a logic 1.
2. Write the High byte address to Derivative Register 08 (Derivative Port 6 latch).
3. Write the Low byte address to Port 0 (Low byte address latch of internal Coding Table).
4. Read Derivative Register 05 (Derivative Port 5 terminal); code data has now been retrieved.
5. Repeat steps 4 and 5 to read more code data.

Table 7 shows a subroutine that reads the Coding Table and then loads code data into system RAM.

Entry:

R0 contains the starting address in system RAM into which data will be loaded.

R1 contains the number of bytes in the Coding Table which are to be read.

R3 holds the Coding Table starting address (Low byte).

R4 holds the Coding Table starting address (High byte).

Exit:

((R0)), ((R0) + 1) $\rightarrow$((R0) + (R1) – 1) contain the code data

Table 7 Subroutine to access the Coding Table

ADDRESS	INSTRUCTION	DESCRIPTION
CODE	ORL P1,#FF	Set all sense lines to logic 1.
	MOV A,R4	Load Accumulator with the High byte of the starting address.
	MOV D8,A	Write the High byte of the starting address to Derivative Port 6 latch.
CODE1	MOV A,R3	Load Accumulator with the Low byte of the starting address.
	OUTL P0,A	Write the Low byte of the starting address to Port 0.
	MOV A,D5	Read code data from Derivative Port 5 terminal into the Accumulator.
	MOV @R0,A	Store code data in system RAM.
	DJNZ R1,CODE2	If more code data is to be read jump to CODE 2, if not go to next instruction.
	RET	Return from subroutine to main program.
CODE2	INC R0	Increment RAM address pointer.
	INC R3	Increment Low byte address of Coding Table.
	JMP CODE1	Jump to CODE 1.

9 WATCHDOG TIMER (WDT)

The PCA84C92X contains a Watchdog Timer that functions in the same manner as the Watchdog Timer used in the PCA84CX22 range of microcontrollers.

The purpose of the Watchdog Timer is to reset the microcontroller if it enters an erroneous processor state; within a reasonable period of time. Erroneous processor states can be caused by noise or RFI.

The Watchdog Timer consists of a 17-bit counter which is clocked at a frequency of $\frac{1}{30}f_{osc}$. During a Power-on-reset the contents of the counter are cleared. The counter contents are then incremented by '1' every 30 cycles of the oscillator clock. If the maximum count is exceeded, the counter overflows and the microcontroller is reset. In order to prevent a counter overflow and its resulting reset operation, the user program must clear the contents of the Watchdog Timer before its maximum count is reached.

During normal processing, the contents of the Watchdog Timer are cleared by writing a logic 1 to the WRES bit in Hardware Modulator Control Register (address 03H).

The maximum time period (t_p) which the counter may run and not cause a reset operation, is calculated as shown below.

$$t_p = \frac{1}{f_{osc}} \times 30 \times 2^{16}$$

In the Idle mode the oscillator is still running and the Watchdog Timer remains active. In the Stop mode however, the oscillator is stopped and the operation of the Watchdog Timer is halted but its contents are retained. Therefore, it may be advisable for the user to clear the contents of the Watchdog Timer before the Stop mode is entered, in order to avoid an unexpected reset operation after the device is woken-up.

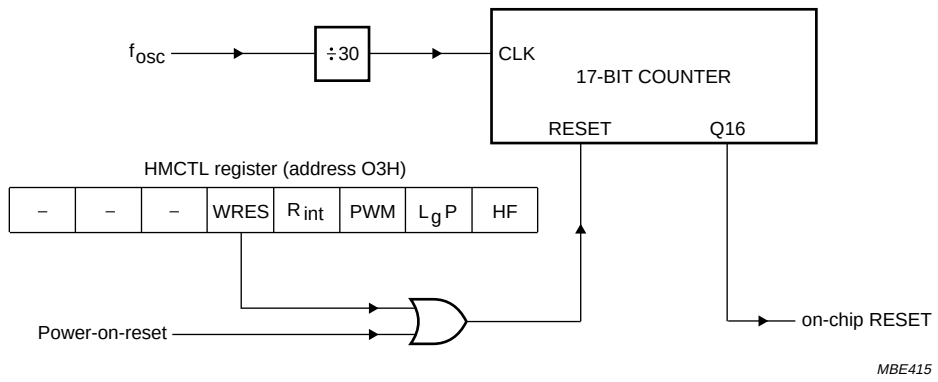


Fig.15 Block diagram of the Watchdog Timer.

10 PORT OPTIONS

Ports can be configured using one of three mask options. The three I/O mask options are specified below.

Option 1 Standard I/O with switched pull-up current source; this is shown in Fig.16.

Option 2 I/O with open-drain output; this is shown in Fig.17.

Option 3 Push-pull output; this is shown in Fig.18.

The state of the ports and the LOUT pin after a Power-on-reset can also be selected using mask options. All mask options are given in Table 8.

Table 8 Mask options

PORT LINES/PIN	S	R	OPTION
P00 to P07			1 or 3; notes 1 and 2
P10 to P13	X		1; note 3
P14 to P17			1; note 3
P20 to P23			
DP50 to DP57	X		1
DP60 to DP67			1 or 3; notes 1, 2 and 4
LOUT	X		2 or 3

Notes to Table 8

1. If diodes are used for system selection the scan lines (Port 0 and Derivative Port 6) cannot take Option 3.
2. Scan lines should have the option ‘1R’.
3. Sense lines should have the option ‘1S’.
4. Only the PCA84C923D has external Derivative Port 6 terminals and therefore this option is only valid for this device. The other members of the range have the state of their internal Derivative Port 6 latch fixed at ‘1S’.

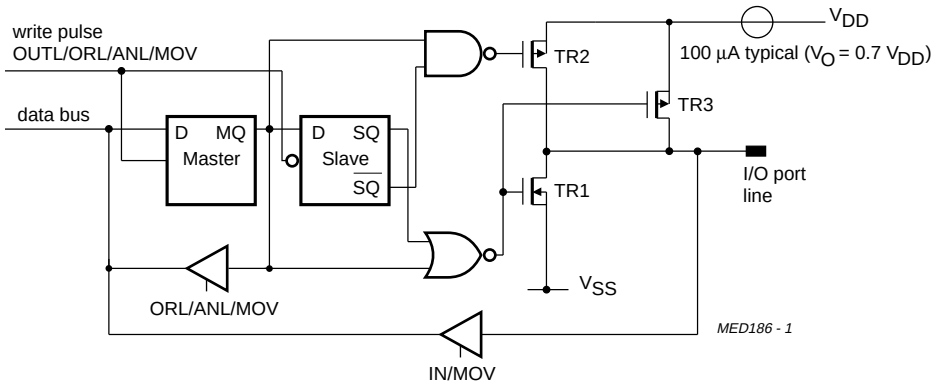


Fig.16 Standard I/O with switched pull-up current source (Option 1).

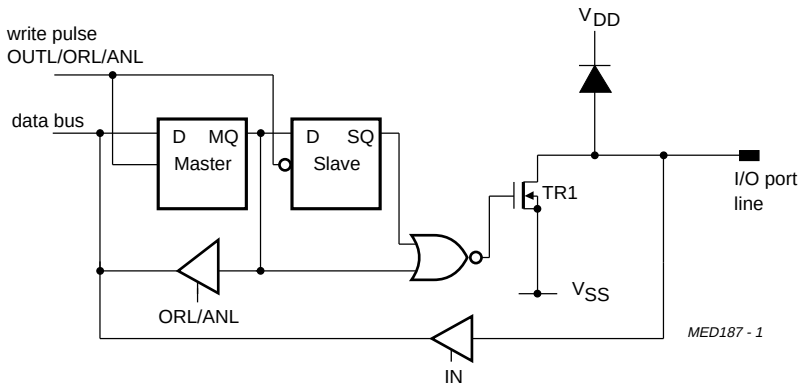


Fig.17 I/O with open-drain output (Option 2).

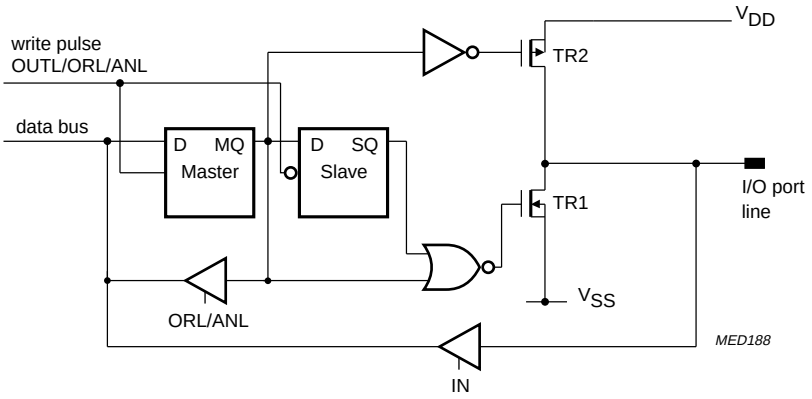


Fig.18 Push-pull output (Option 3).

11 INTERRUPTS

The PCA84C92X has three interrupt sources:

1. External keypad wake-up and T0/$\overline{\text{INT}}$ pin; vector address 03H.
2. Hardware Modulator; vector address 05H.
3. Internal Timer/counter (T1); vector address 07H.

11.1 External keypad wake-up and T0/$\overline{\text{INT}}$ pin interrupt

This interrupt will wake-up the CPU from the Stop mode when a HIGH-to-LOW transition occurs on any Port 1 pin or the T0/$\overline{\text{INT}}$ pin (see Fig.1); normal program execution will continue after a 1866 clock cycle delay.

If this interrupt was enabled (by using the 'EN I' instruction) before the Stop mode was entered, then when the CPU is woken-up, the instruction that follows the STOP instruction will be executed before diverting to the interrupt routine at vector address 03H. However, if the interrupt was not enabled before the Stop mode was entered, then when the CPU is woken-up the instruction that follows the STOP instruction will be executed.

11.2 Hardware Modulator interrupt

When a complete pulse train has been transmitted by the Hardware Modulator, it generates an interrupt to the CPU by asserting $\overline{\text{EXDI}}$ and the operation of the Hardware Modulator is halted. This derivative interrupt is shared with the SIO interrupt of the PCF84CXXXA family; both use vector address 05H. The Hardware Modulator interrupt is enabled using the instruction 'EN SI' and is disabled using the 'DIS SI' instruction.

11.3 Internal Timer/counter (T1) interrupt

The Timer/counter and its interrupt are common to other members of the PCF84CXXXA family; all operate in a similar manner. The Timer/counter interrupt is enabled using the instruction 'EN TCNT1' and is disabled using the 'DIS TCNT1' instruction.

12 DERIVATIVE REGISTERS

The Derivative Registers residing at addresses 00 to 04H are dedicated to the Hardware Modulator; these registers are also common to the PCA84CX22 range of microcontrollers. The Derivative Registers residing at addresses 05 to 08H are used for accessing the Coding Table. The Derivative Registers memory map is shown in Table 9.

When the Coding Table is accessed data will be read from Derivative Port 5 terminal (address 05H) regardless of whether the internal or external Coding table was addressed. Details of accessing the internal or external Coding Tables are given in Section 8. As Derivative Port 6 latch is also connected to the High byte address of the internal Coding Table, writing data to Derivative Port 6 latch (address 08H) also addresses the Coding Table.

Table 9 Derivative Registers memory map (see note 1)

ADDR (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	ON-TIME	ON7 (X)	ON6 (X)	ON5 (X)	ON4 (X)	ON3 (X)	ON2 (X)	ON1 (X)	ON0 (X)	R/W
01	OFF-TIME	OFF7 (X)	OFF6 (X)	OFF5 (X)	OFF4 (X)	OFF3 (X)	OFF2 (X)	OFF1 (X)	OFF0 (X)	R/W
02	Pulse Counter Low (PULOW)	PUL7 (X)	PUL6 (X)	PUL5 (X)	PUL4 (X)	PUL3 (X)	PUL2 (X)	PUL1 (X)	PUL0 (X)	R/W
03	Hardware Modulator Control (HMCTL)	–	–	–	WRES(2) (X)	Rint(2) (X)	PWM (X)	LgP (X)	HF (X)	R/W
04	Pulse Counter High (PUHIGH)	–	–	–	–	–	–	PUL9 (X)	PUL8 (X)	R/W
05	Derivative Port 5 (terminal)	DP57/MD7 (X)	DP56/MD6 (X)	DP55/MD5 (X)	DP54/MD4 (X)	DP53/MD3 (X)	DP52/MD2 (X)	DP51/MD1 (X)	DP50/MD0 (X)	R
06	Derivative Port 6 (terminal)	DP67 (X)	DP66 (X)	DP65 (X)	DP64 (X)	DP63 (X)	DP62 (X)	DP61 (X)	DP60 (X)	R
07	Derivative Port 5 (latch)	DP57 (1)	DP56 (1)	DP55 (1)	DP54 (1)	DP53 (1)	DP52 (1)	DP51 (1)	DP50 (1)	R/W
08	Derivative Port 6 (latch)	DP67/MA15 (Mo)	DP66/MA14 (Mo)	DP65/MA13 (Mo)	DP64/MA12 (Mo)	DP63/MA11 (Mo)	DP62/MA10 (Mo)	DP61/MA9 (Mo)	DP60/MA8 (Mo)	R/W

Notes

1. Values within parethesis show the bit state after a reset operation. ‘X’ denotes an undefined state and ‘Mo’ denotes the state is selected by mask option.
2. These bits are Write only.

13 EMULATION

The PCA84C923D can be used as the emulation chip for both the PCA84C92X and PCA84CX22 ranges of microcontrollers. The emulation system is shown in Fig.19.

A 64 kbyte EPROM (27C256) is used as the Coding Table and stores all data code. The EPROM should be removed when members of the PCA84CX22 range are being emulated.

The PCA84C923D has two additional outputs: $\overline{\text{INTO}}$ and RSTO which are used for emulation purposes only. The $\overline{\text{INTO}}$ output is the result of the AND operation carried out internally on the T0/$\overline{\text{INT}}$ and Port 1 inputs; this is shown in Fig.1. The RSTO output is the result of the OR operation carried out internally on the RESET input and the Watchdog Timer reset; this is also shown in Fig.1. The $\overline{\text{INTO}}$ and RSTO pins of the PCA84C923D are connected to the T0/$\overline{\text{INT}}$ and RESET pins of the bond-out chip, respectively.

The RESET and T0/INT inputs are connected to the corresponding pins of the PCA84C923D (in other 84CXXX emulation systems they are connected to the corresponding pins of the PCF84C00).

In the emulation mode, port lines P10 to P13 of the PCA84C923D are used as the inputs for derivative control signals $\overline{\text{DXWR}}$, $\overline{\text{DXRD}}$, DXALE and EXDIN. Therefore, port lines P20 to P23 (which are ANDed internally to emulate the wake-up function of port lines P10 to P13) are connected to port lines P10 to P13 of the bond-out chip. If port lines P14 to P17 of the PCA84C923D have been masked for the wake-up function, then they must not be connected to the corresponding pins of the bond-out chip. However, these sets of pins can be connected if the wake-up option has not been selected.

When the PCA84C923D is used as the emulation chip all ports should have the mask option 1S. After a Power-on-reset the only data that can be written to Derivative Port 5 is FFH.

When the PCF84C00 is used for emulation purposes its ports should have the mask option 1S. However, as some ports may be used as scan lines (for example Port 1 and Port 6) they will have mask options of 1R or 3R. In this case, after a Power-on-reset, these ports should have 00H written to them.

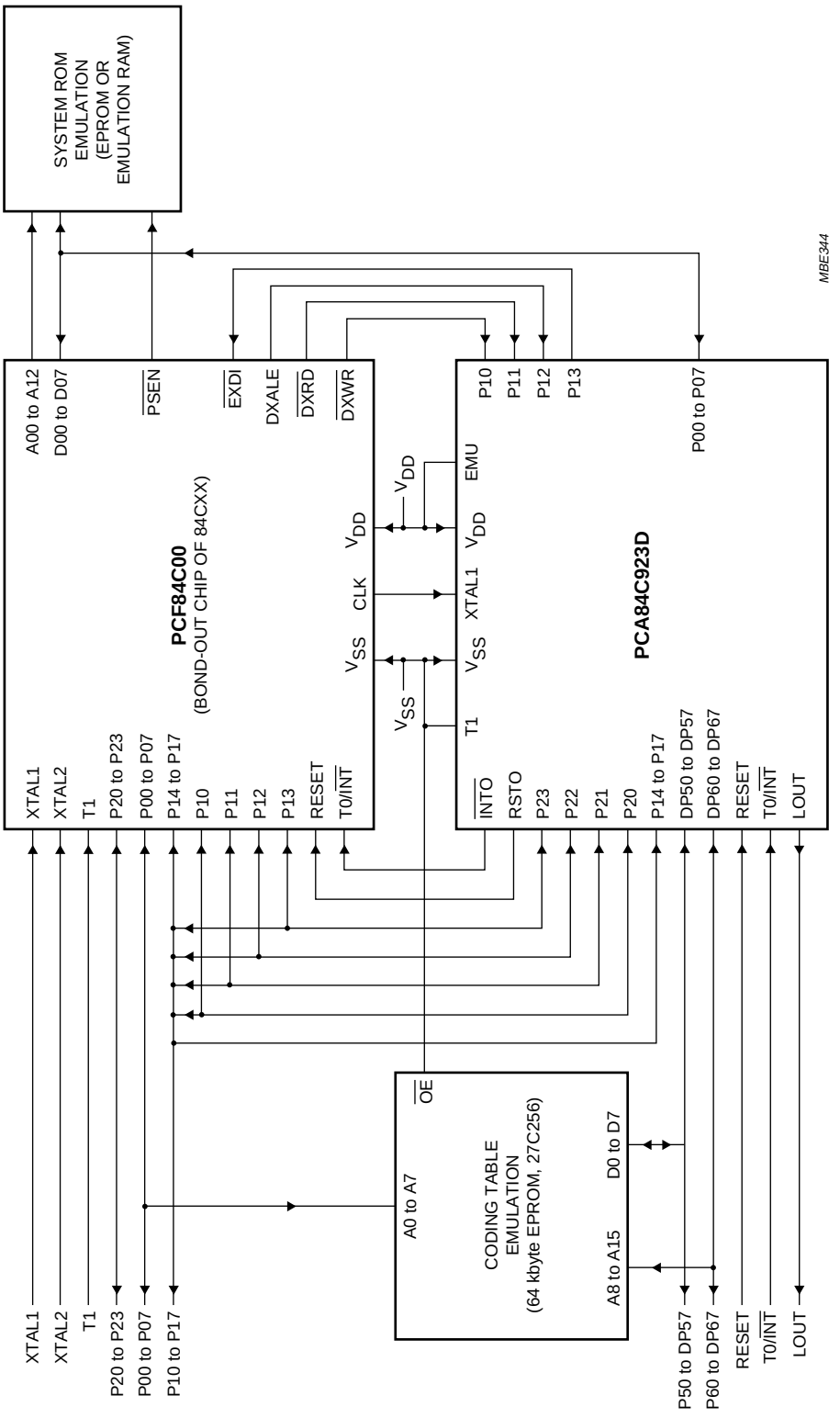


Fig.19 Emulation circuit of PCA84C922 and PCA84C923.

14 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 34).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7.0	V
V_I	all input voltages on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
I_{OH}	maximum source current for all port lines	–	–5.0	mA
I_{OL}	maximum sink current for all port lines	–	5.0	mA
P_{tot}	total power dissipation	–	500	mW
T_{amb}	operating ambient temperature	–20	+70	°C
T_{stg}	storage temperature	–55	+125	°C

15 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = −25 to +50 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.0	3.0	5.5	V
I_{DD}	operating supply current	V_{DD} = 3 V; f_{xtal} = 3 MHz	–	0.4	0.9	mA
		V_{DD} = 5 V; f_{xtal} = 3 MHz	–	0.9	1.8	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 3 V; f_{xtal} = 3 MHz	–	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 3 MHz	–	0.25	0.5	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 2 V; T_{amb} = 25 °C; note 1	–	1.2	2.4	µA
		V_{DD} = 2 V; T_{amb} = 50 °C; note 1	–	–	10.0	µA
		V_{DD} = 3 V; T_{amb} = 25 °C; note 1	–	1.2	2.4	µA
		V_{DD} = 3 V; T_{amb} = 50 °C; note 1	–	–	10.0	µA
		V_{DD} = 5 V; T_{amb} = 25 °C; note 1	–	1.2	2.4	µA
		V_{DD} = 5 V; T_{amb} = 50 °C; note 1	–	–	10.0	µA
Inputs EMU; RESET; T0/INTN; T1; P00 to P07; P!0 to P17; P20 to P23; DP50 to DP57 and DP60 to DP67						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$	–	–	±1	µA
Outputs P00 to P07; P10 to P17; DP50 to DP57; DP60 to DP67; INTN0 and RSTO						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_O = 0.4 V	–	12	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	−40	−100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	−140	−400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ − 0.4 V	–	−7.0	–	mA
Outputs P20 to P23						
I_{OL}	LOW level output sink current	V_{DD} = 3 V; V_O = 0.4 V	10	–	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	−40	−100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	−140	−400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ − 0.4 V	–	−7.0	–	mA
Output LOUT						
I_{OL}	LOW level output sink current	V_{DD} = 2 V; V_O = 1 V	30	–	–	mA
I_{OH}	HIGH level output source current	V_{DD} = 2 V; V_O = 1.6 V	−1.6	–	–	mA

Note

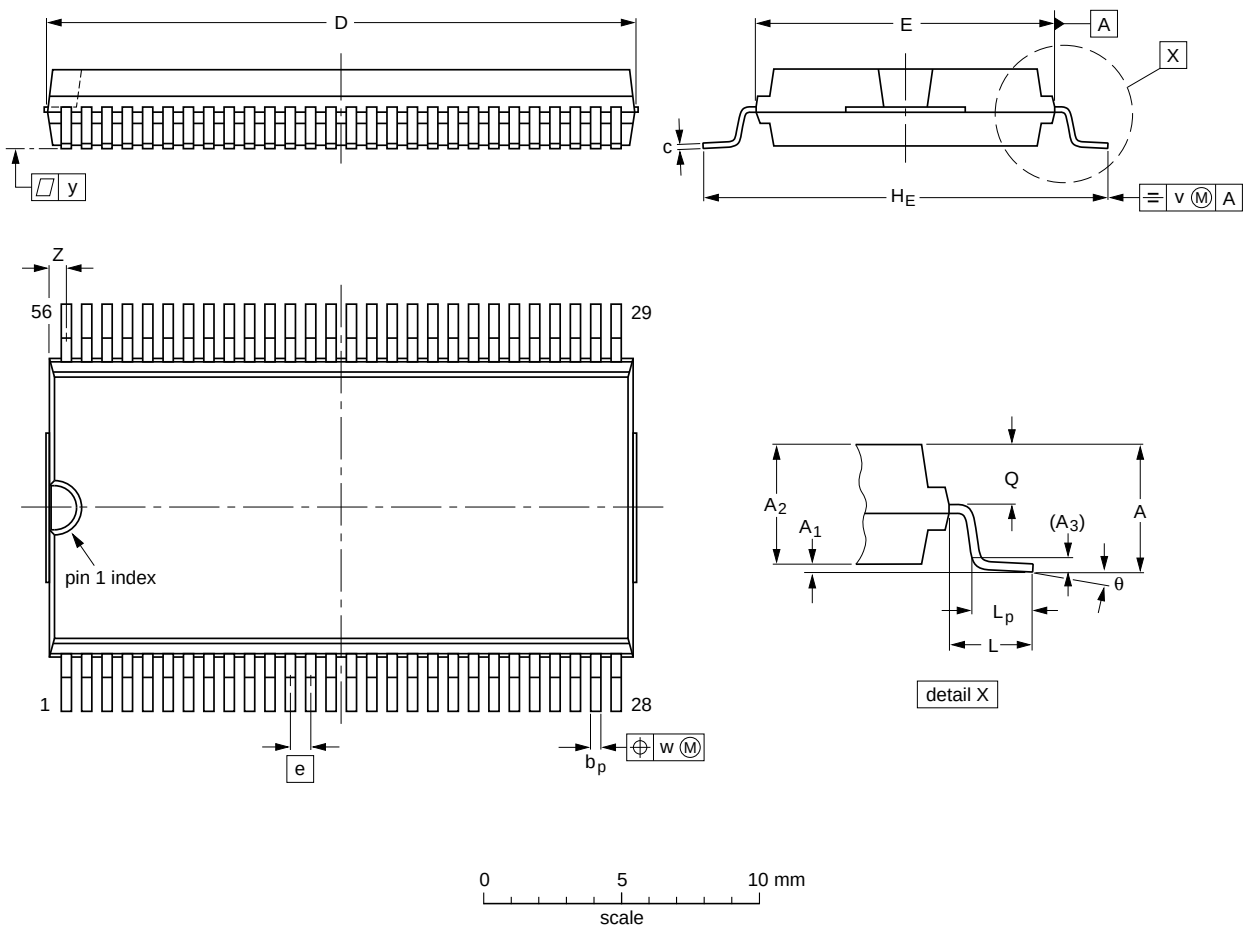
1. f_{xtal} = 3 MHz.

16 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	crystal oscillator frequency	V_{DD} = 2.5 to 5.5 V	1	–	6	MHz
		V_{DD} = 2 to 5.5 V	1	–	4.5	MHz
Transconductance						
g_{mL}	option LOW	V_{DD} = 5 V	0.3	0.7	1.4	mS
g_{mM}	option MEDIUM	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	option HIGH	V_{DD} = 5 V	3	4.5	9.0	mS
Rf	feedback resistor		0.3	1	3	MΩ

17 PACKAGE OUTLINES

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

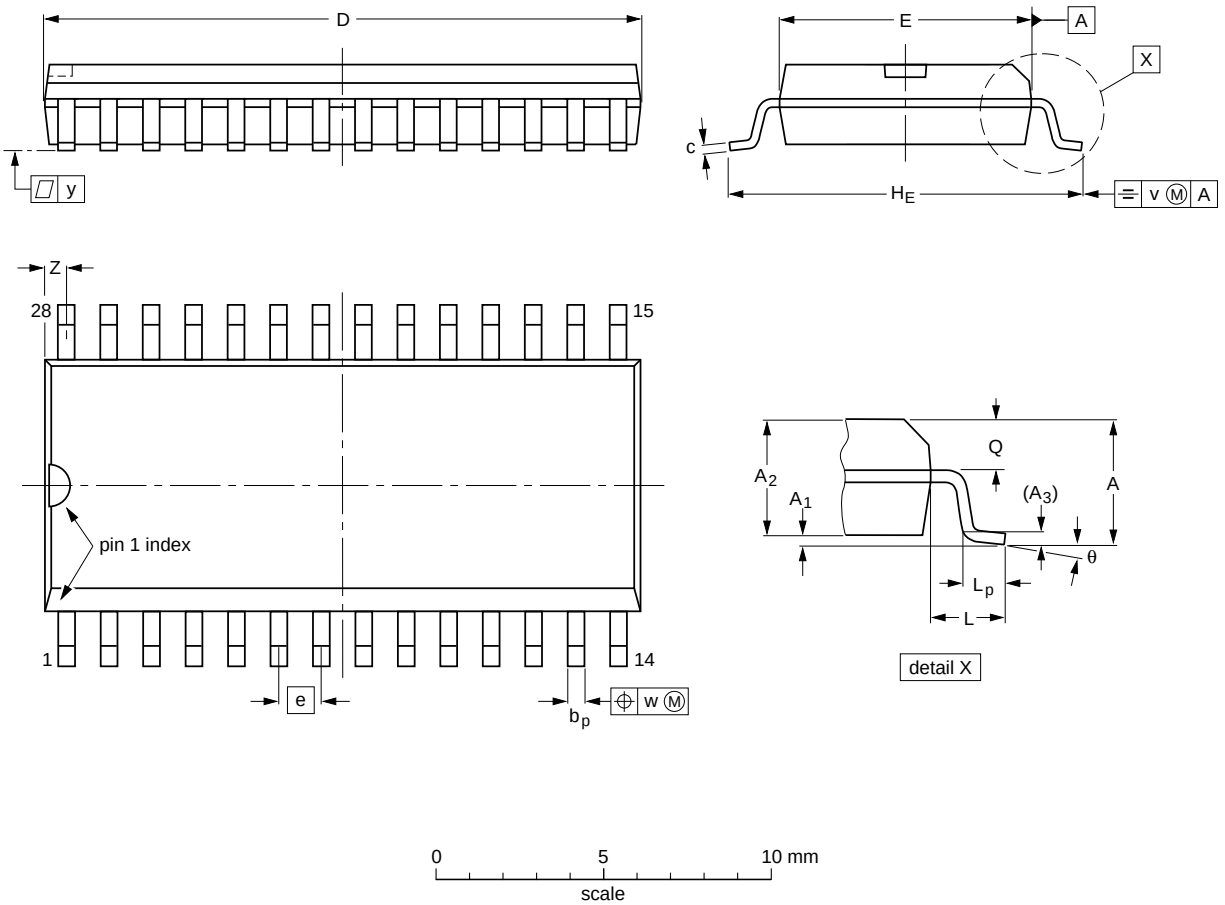
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.9 21.5	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7^o 0^o
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0085	0.86 0.55	0.44 0.43	0.03	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~92-11-17~~ 95-01-24

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

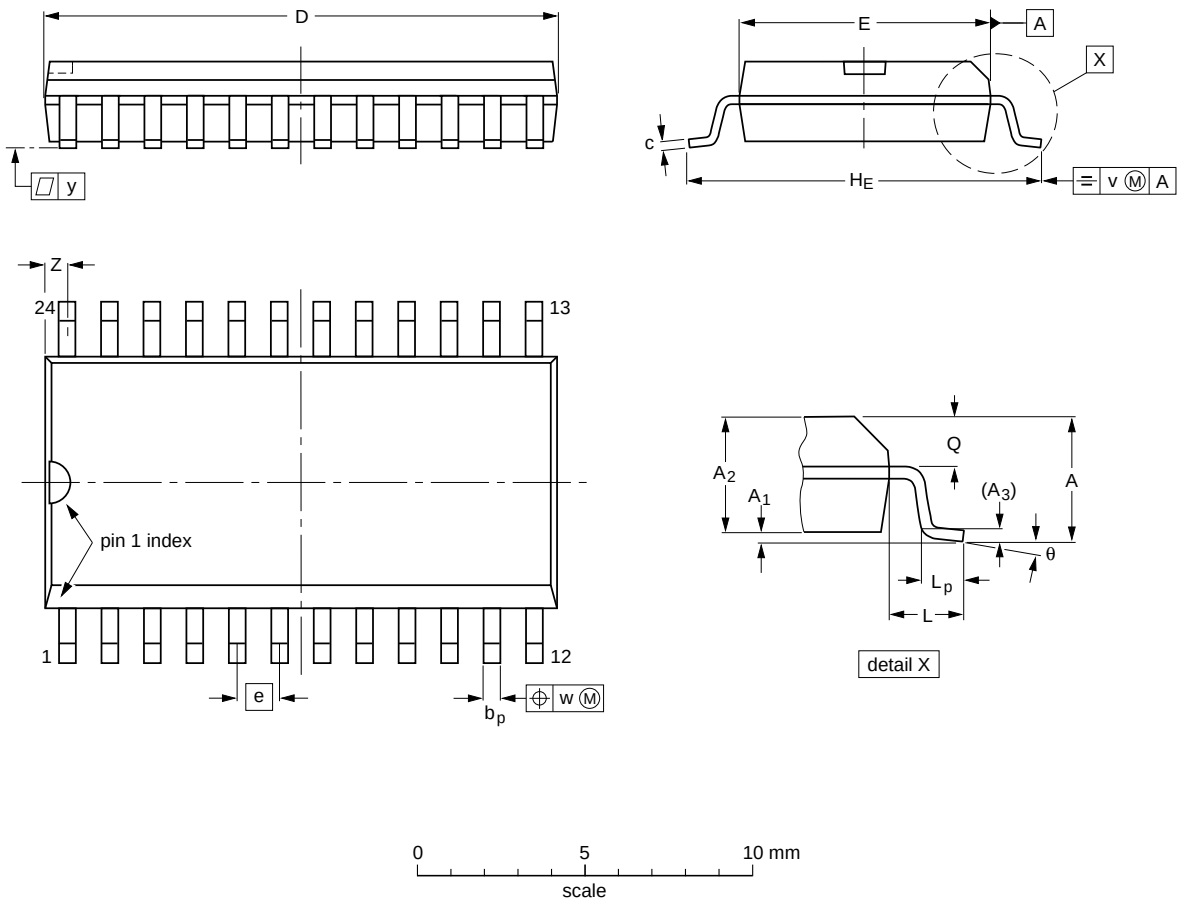
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

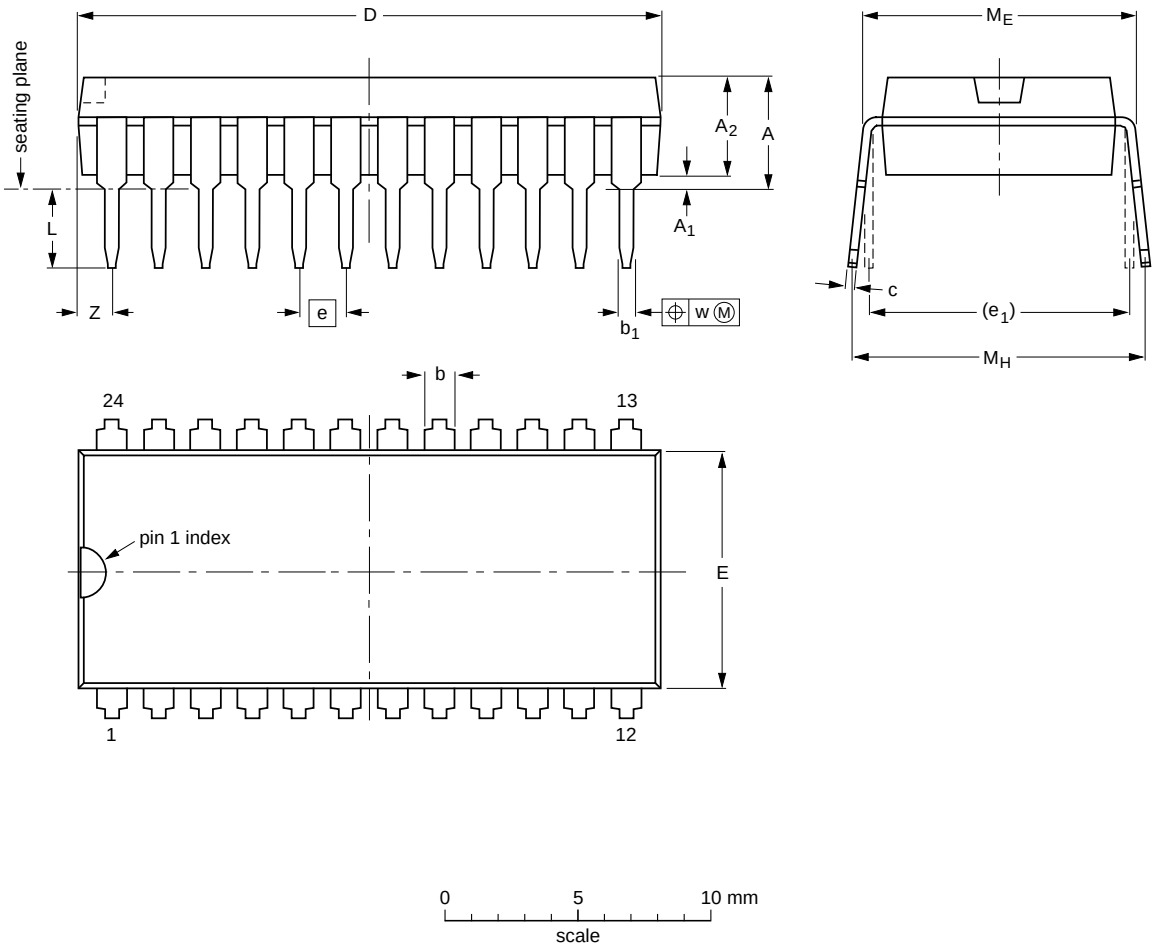
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

18.2 SDIP

18.2.1 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

18.2.2 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

18.3 SO and VSO

18.3.1 Reflow soldering

Reflow soldering techniques are suitable for all SO and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

18.3.2 Wave soldering

Wave soldering techniques can be used for all SO and VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.3.3 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

20 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

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